Title: **SEMICONDUCTOR DEVICE WITH LIGHTLY DOPED DRAIN AND METHOD OF MANUFACTURING THE SAME**

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Cross Reference to Related Applications

[0001] This application claims priority to Taiwan Patent Application No. 091124959 entitled "Semiconductor Device with Lightly Doped Drain and Manufacturing Method thereof", filed on October 25, 2002.

Field of Invention

[0002] The present invention relates to a semiconductor device and its manufacture method, and more particularly, to a thin film transistor with lightly doped drain (LDD) and a method of manufacturing the same.

Background of the Invention

[0003] Semiconductor devices generally have lots of circuits and devices to control their functions, and the thin film transistor (TFT) is one of the most commonly implemented devices. For example, in the liquid crystal display (LCD) device, the thin film transistors are often used as pixel switching elements, or switches in a driver circuit.

[0004] However, as the channel length of thin film transistors keeps on shrinking, the short channel effect seriously affects the operation of the thin film transistors. For example, the high electric field near the drain of TFT usually induces high leakage currents. Therefore, lightly doped drain (LDD) structure, offset gate structure, or multi-gate structure are conventionally implemented by designers to suppress the high electric

field. The lightly doped drain technique, among others, is most commonly adopted to reduce the leakage current when the transistor is at ON state.

[0005] The conventional method of forming a lightly doped structure usually needs extra masks, which increases the production cost and complicates the manufacturing process. For example, in the conventional method, the photolithography process usually defines the LDD length. When misalignment occurs in the photolithography process, a variation in the LDD length is induced. Therefore, it is important to reduce the number of masks and improve the alignment accuracy of the photolithography process in manufacturing TFT-LCD devices.

[0006] As disclosed in U.S. Patent No. 6,306,693, the conventional method performs a first n-type-doping step after the gate electrode of the n-typed transistor is etched. Then, the patterned mask layer used for forming the gate electrode is left and used to perform side etching of a portion of the gate electrode, and then is removed. The side-etched gate electrode is then used as a mask to perform a second n-type-doping step to define the lightly doped region, and therefore the number of masks is reduced. However, the result of side etching (or undercut etching) process is difficult to control, which induces a variation in the amount of side etching of the gate electrode. As a result, the subsequent doping step creates a variation in the LDD length. Therefore, it is desired to provide a method of simplified step for forming a semiconductor device with a uniform LDD length.

Summary of the Invention

[0007] It is one aspect of the present invention to provide a semiconductor device with lightly doped drain (LDD). The semiconductor device has a spacer serving as a hard mask to prevent variations in the LDD length during the formation of LDDs.

[0008] It is another aspect of the present invention to provide a method of manufacturing a semiconductor device, which eliminates variations in the LDD length induced by misalignment of the photolithography process.

[0009] It is a further aspect of the present invention to provide a method of forming a thin film transistor, which implements a spacer as a selfaligned hard mask to prevent deviations of a patterned photoresist layer.

[0010] It is a further another aspect of the present invention to provide a method of forming driver/control circuits of a liquid crystal display (LCD), which uses simplified processing steps to form devices with lightly doped drains in the process of forming a spacer and gate electrodes of different conduction type transistors.

[0011] In one exemplary embodiment, the method includes the step of providing a semiconductor substrate having a first area and a second area for respectively forming a first conduction type thin film transistor and a second conduction type thin film transistor. A gate dielectric layer is formed on the semiconductor substrate, and a conductive layer is formed on the gate dielectric layer. A portion of the conductive layer is selectively removed to form a first gate electrode on the gate dielectric layer, which corresponds to the first area. A portion of remains of the conductive layer substantially overlies the second area. A first impurity of a first conduction type is doped in the first area. A spacer is formed on a sidewall of the first gate electrode. A second impurity of first conduction type is doped in the first area to form the first conduction type transistor. A patterned mask layer is formed over the semiconductor substrate. The patterned mask layer defines a second gate electrode of the conductive layer, which corresponds to the second area. A portion of the conductive layer, which corresponds to the second area, is removed to form the second gate electrode on the gate dielectric layer by using the patterned mask layer as

a mask. An impurity of a second conduction type is doped in the second area to form the second conduction type transistor.

[0012] In another exemplary embodiment, a semiconductor device with a lightly doped region includes a semiconductor substrate having a first area and a second area, a first type transistor formed in the first area, and a second type transistor formed in the second area. Each of the first type and second type transistors includes source/drain regions, a gate dielectric layer, and a gate electrode. The source/drain regions are formed in the semiconductor substrate and separated by a channel. The gate dielectric layer is formed on the semiconductor substrate covering the channel. The gate electrode is formed on the gate dielectric layer corresponding to the channel. The first type transistor further includes a spacer and a lightly doped region. The spacer is formed on a sidewall of the gate electrode and on the gate dielectric layer corresponding to the first area. The lightly doped region is formed in a portion of the source/drain region corresponding to the spacer.

Brief Description of the Drawings

[0013] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0014] Fig. 1 illustrates a cross-sectional view of forming a conductive layer in one exemplary embodiment of the present invention;

[0015] Fig. 2 illustrates a cross-sectional view of forming a patterned photoresist layer defining a first gate electrode in one exemplary embodiment of the present invention;

[0016] Fig. 3 illustrates a cross-sectional view of forming a first gate electrode in one exemplary embodiment of the present invention;

[0017] Fig. 4 illustrates a cross-sectional view of implanting first n-type ions in one exemplary embodiment of the present invention;

[0018] Fig. 5 illustrates a cross-sectional view of forming a conformal dielectric layer in one exemplary embodiment of the present invention;

[0019] Fig. 6 illustrates a cross-sectional view of implanting second n-type ions in one exemplary embodiment of the present invention;

[0020] Fig. 7 illustrates a cross-sectional view of a patterned photoresist layer defining a second gate electrode in one exemplary embodiment of the present invention;

[0021] Fig. 8 illustrates a cross-sectional view of implanting p-type ions in one exemplary embodiment of the present invention; and

[0022] Fig. 9 illustrates a cross-sectional view of a semiconductor device with n-type and p-type thin film transistors in another exemplary embodiment of the present invention.

Detailed Description of the Invention

[0023] A semiconductor device with a lightly doped drain and a method of manufacturing the semiconductor device are provided to eliminate variations in the LDD length and simplify the manufacturing process. In one exemplary embodiment of the present invention, a method of forming a semiconductor device, such as driver/control circuits of LCD device, is illustrated. As shown in Fig. 1, the method includes steps of providing a semiconductor substrate 100, such as a silicon substrate, a silicon layer formed on an insulating layer, or a layer of any semiconductor material as appropriate. The semiconductor substrate 100 includes a first area 110 and a second area 120 for respectively forming a first type transistor and a second type transistor, such as an n-type thin film transistor and a p-type thin film transistor.

[0024] As shown in Fig. 1, the exemplary substrate 100 is a silicon layer 102 formed on an insulating layer 104, which includes an oxide layer formed on a quartz or glass substrate (106). The first area 110 is shown in the driver area 200 or the pixel area 300 of the semiconductor device. The second area 120 is shown in the driver area 200 of the semiconductor device.

[0025] Then, a gate dielectric layer 112 is formed on the substrate 100. The gate dielectric layer 112, which is selected form the group consisting of a nitride layer, an oxide layer, and a combination thereof, can be formed by the thermal oxidation technique or the deposition technique. A conductive layer 114 is subsequently formed on the gate dielectric layer 112. The conductive layer 114 can be a polysilicon layer or a layer of any conductive material and formed by the deposition technique. Then, a portion of the conductive layer 114 is selectively removed to form a first gate electrode 118 on the gate dielectric layer 112, which corresponds to the first area 110, and a portion of remains of the conductive layer 114 substantially overlies the second area 120, as shown in Fig. 3.

[0026] Referring to Fig. 2, the step of selectively removing the conductive layer 114 to form the first gate electrode 118 includes the step of forming a photoresist layer 116 on the conductive layer 114. The photoresist layer 116 is patterned to define the first gate electrode 118 of the conductive layer 114 corresponding to the first area 110. The formation of the patterned photoresist layer 116 can be achieved by a convention photolithography technique including coating, exposure, and development processes. As shown in Fig. 3, the conductive layer 114 is etched to expose the gate dielectric layer 112 by using the patterned photoresist layer 116 as a mask, so that a first portion of the conductive layer 114 forms the first gate electrode 118, and a second portion of the conductive layer 114 substantially overlies the second area 120. It is noted that the

remains of the photoresist layer 116 is removed after the formation of the first gate electrode 118.

[0027] As shown in Fig. 4, a first impurity of a first conduction type is doped in the first area 110 by using the patterned transferred conductive layer as a mask. For example, the first n-type dopants are ion-implanted into the silicon layer 102 in the first area 110 to form at least one lightly doped region 122 by using the gate electrode 118 and the remains of the conductive layer 114 as a mask. The first n-type dopants can be selected from the group consisting of phosphorous, arsenic, and the like as appropriate.

[0028] As shown in Figs. 5 and 6, a conformal dielectric layer 124 is formed over the semiconductor substrate 100 and then anisotropically etched to form a spacer 126 on the sidewall of the first gate electrode 118. Then, a second impurity of the first conduction type is doped on the first area. For example, the second n-type dopants are ion-implanted into the silicon layer 102 in the first area 110 to form at least one heavy doped region 128 by using the first gate electrode 118 and the spacer 126 as a mask. The heavy doped region 128 adjacent to a portion of the lightly doped region 122. Therefore, the lightly doped drain 122 formed in the n-type transistor has the same length due to the symmetrical feature of the spacer 126 as shown in Fig. 6. The second n-type dopants can be selected from the group consisting of phosphorous, arsenic, and the like as appropriate. It is noted that the first and second impurities of the first conduction type can be two different doping materials or the same doping material. For example, the first and second n-type dopants can both be phosphorous, or respectively be phosphorous and arsenic.

[0029] As shown in Fig. 7, a patterned mask layer 130, which defines a second gate electrode 132 of the conductive layer 114 corresponding to the second area 120, is formed over the semiconductor substrate 100. As shown in Fig. 8, a portion of the conductive layer 114, which corresponds to the second area 120, is etched to form the second

electrode 132 on the dielectric layer 112 corresponding to the second area 120 by using the patterned mask layer 130 as a mask. As also shown in Fig. 8, an impurity of a second conduction type is doped in the second area 120 of the semiconductor substrate 110. For example, p-type dopants are ion-implanted in into the silicon layer 102, which corresponds to the second area 120, to form at least one doped region 134 by using the patterned mask layer 130 as a mask to form the p-type transistor. Then, the patterned mask layer 130 is removed as shown in Fig. 9.

[0030] The method further includes the steps of forming capacitors, contacts, wire circuits, and pixel contacts (not shown) to accomplish the formation of driver/pixel-control circuits of an LCD device. Furthermore, though the exemplary embodiment is illustrated to form driver/pixel-control circuits of LCD devices, it is noted that the method can be implemented to form other semiconductor devices with lightly doped drain.

[0031] A shown in Fig. 9, in another exemplary embodiment, a semiconductor device 400 with a lightly doped region 122 is also provided. The semiconductor device 400 includes a semiconductor substrate 100 having a first area 110 and a second area 120, a first type thin film transistor 410 formed in the first area 110, and a second type thin film transistor 420 formed in the second area 120. As described above, the semiconductor substrate 100 can be a silicon substrate, or a substrate having a silicon layer 102 formed on an insulating layer 104 and a quartz or glass substrate 106. The first type thin film transistor 410 and the second type thin film transistor 420 can respectively be an n-type thin film transistor and a p-type thin film transistor shown in the driver area 200 or the pixel area 300.

[0032] The first type thin film transistor 410 includes first source/drain regions 412 formed in the semiconductor substrate 100 and separated by a first channel 414. The first gate dielectric layer 112, which is formed on the semiconductor substrate 100, covers the first channel 414. The first gate electrode 118, which is formed on the first gate dielectric

layer 112, corresponds to the first channel 414. A spacer 126 is formed on a sidewall of the first gate electrode 118 and on the first gate dielectric layer 112. A lightly doped region 122, which is formed in a portion of the source/drain region 412, corresponds to the spacer 126. In other words, the first source/drain region 412 includes a heavy doped region 128 and a lightly doped region 122.

[0033] The second type thin film transistor 420 includes second source/drain regions 134 formed in the semiconductor substrate 100 and separated by a second channel 422. The second gate dielectric layer 112 is formed on the semiconductor substrate 100 to cover the second channel 422. The second gate electrode 132, which is formed on the second gate dielectric layer 112, corresponds to the second channel 422. As shown in Fig. 9, the first gate dielectric layer and the second gate dielectric layer formed at the same time is the gate dielectric layer 112. The second source/drain regions are the doped regions 134.

[0034] Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.